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(71)Applicant : NEC CORP

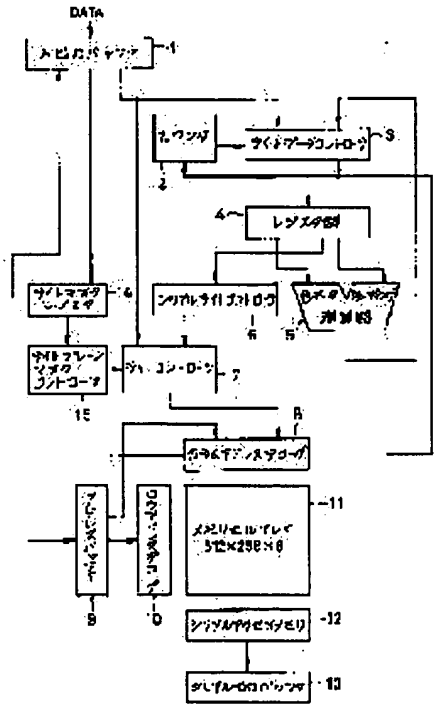
(72)Inventor : ITO TARO

(54) PICTURE PROCESSOR

(57)Abstract:

PURPOSE: To make the device compact by attaining the sufficiently fast processing speed when plotting the picture by using the shading technic and reducing the parts cost and the parts mounting area.

CONSTITUTION: A write data controller 3 stores only the color data of the respective picture elements at the plotting start point and the plotting end point in the register of a register group 4 corresponding to the column address from a column address decoder 8. A color data shading arithmetic device 5 performs shading by linearly complementing the color data at the plotting start point and the color data of the plotting end point. The color data of the picture element which is shaded by the arithmetic device 5 is written successively in the corresponding register in the register group 4 by the write data controller 3. The data of the register group 4 are written in a memory cell array 11 by a max. amt. of 256 picture elements at the same time by a serial write controller 6.



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(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目7番1号

(72)発明者　伊東　太郎
東京都港区芝五丁目7番1号　日本電気株式会社内

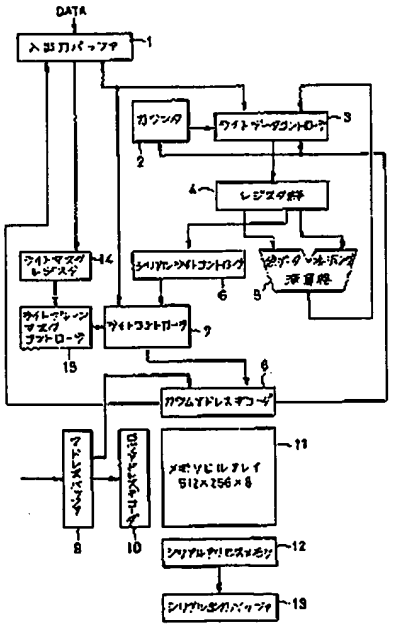
(74)代理人　弁理士　▲柿▼川　信

(54)【発明の名称】　画像処理装置

(57)【要約】

【目的】　シェーディングの手法を用いて画像を描画する際に充分な処理速度を得るとともに、部品コスト及び部品実装面積を低減して装置の小型化を可能とする。

【構成】　ライトデータコントローラ3はカラムアドレスデコーダ8からのカラムアドレスに対応するレジスタ群4のレジスタに描画開始点及び描画終了点各々の画素の色データのみをストアする。色データシェーディング演算器5は描画開始点の色データと描画終了点の色データとを線形補完することでシェーディングを行う。色データシェーディング演算器5でシェーディングされた画素の色データはライトデータコントローラ3によってレジスタ群4の対応するレジスタに順次書込まれていく。レジスタ群4のデータはシリアルライトコントローラ6によって最大256画素分同時にメモリセルアレイ11に書込まれる。



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【特許請求の範囲】

【請求項1】　各々色情報をもつ画素データ列を記憶する画像記憶素子を含む画像処理装置であって、前記画素データ列の色情報を保持する保持手段と、前記保持手段に保持された画素データ列の色情報のうち指定された画素データ各々の色情報を予め設定された方向に順次可変する色情報可変手段と、前記色情報可変手段で可変された色情報を前記保持手段に書込む書込み手段と、前記保持手段の内容を複数の画素データ列の色情報を格納するメモリセルに転送する手段とを前記画像記憶素子に有することを特徴とする画像処理装置。

【請求項2】　前記書込み手段による前記色情報可変手段で可変された色情報を前記保持手段に書込む際に外部から指定された画素データの色情報の書込みを禁止する手段を前記画像記憶素子に含むことを特徴とする請求項1記載の画像処理装置。

【請求項3】　前記書込み手段による前記色情報可変手段で可変された色情報を前記保持手段に書込む際に前記色情報を構成するビット情報のうち外部から指定されたビット情報の書込みを禁止する手段を前記画像記憶素子に含むことを特徴とする請求項1または請求項2記載の画像処理装置。

【請求項4】　前記色情報可変手段は、前記指定された画素データの色情報うち描画開始点となる画素データの色情報及び描画終了点となる画素データの色情報に基づいて前記描画開始点と前記描画終了点との間の画素データ各々の色情報を順次可変するよう構成されたことを特徴とする請求項1から請求項3のいずれか記載の画像処理装置。

【請求項5】　前記色情報可変手段は、前記描画開始点となる画素データの色情報と前記描画終了点となる画素データの色情報との減算を行う減算手段と、前記減算手段の減算結果を前記描画開始点と前記描画終了点との間の画素数で除算する除算手段と、前記除算手段の除算結果を隣合う画素データの色情報に加算する加算手段とから構成されたことを特徴とする請求項4記載の画像処理装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は画像処理装置に関し、特に画像データを高速にメモリセルに書込む必要のある装置に用いられる半導体画像記憶素子に関する。

【0002】

【従来の技術】従来、コンピュータグラフィックスの分野では画像をよりリアルに表現するためにシェーディングモデルが用いられている。このシェーディングモデルとは三次元空間の中に物体や光源があるとき、物体の各点がどのような色や明るさに見えるかを近似的に計算する方式である。

【0003】すなわち、画像が徐々に明るくなっていく

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場合や暗くなっていく場合、あるいは画像の色が徐々に濃くなっていく場合や薄くなっていく場合に、それを表現するためにシェーディングの手法が用いられる。

【0004】このシェーディングの手法では画像の明るさや暗さ、あるいは色の濃さを画像データに対して1画素ずつ計算しており、その計算はソフトウェアまたは外部のハードウェアを用いて行われている。

【0005】これらソフトウェアまたは外部のハードウェアの計算結果は、行アドレスストローブ信号及び列アドレスストローブ信号の立下りのタイミングで決定されるアドレスによって画素の色データを一画素分ずつ画像記憶素子のメモリに記憶している。

【0006】

【発明が解決しようとする課題】上述した従来の画像記憶素子では、シェーディングの手法を用いたソフトウェアまたは外部のハードウェアの計算結果である画素の色データのみが記憶されているが、ソフトウェアにより上記の計算を行い、その計算結果をメモリに記憶する方法の場合、上記の計算に多大な計算コストがかかるため、メモリのアクセス速度を高速化しても、シェーディングの手法を用いて画像を描画する際に充分な処理速度を得ることができない。

【0007】また、外部のハードウェアにより上記の計算を行い、その計算結果をメモリに記憶する方法の場合、上記の計算を行うために多大な部品コスト及び広い部品実装面積が要求されるので、これらが装置を小型化する際の大きな障害となっている。

【0008】そこで、本発明の目的は上記の問題点を解消し、シェーディングの手法を用いて画像を描画する際に充分な処理速度を得ることができ、部品コスト及び部品実装面積を低減して装置の小型化を可能とすることができる画像処理装置を提供することにある。

【0009】

【課題を解決するための手段】本発明による画像処理装置は、各々色情報をもつ画素データ列を記憶する画像記憶素子を含む画像処理装置であって、前記画素データ列の色情報を保持する保持手段と、前記保持手段に保持された画素データ列の色情報のうち指定された画素データ各々の色情報を予め設定された方向に順次可変する色情報可変手段と、前記色情報可変手段で可変された色情報を前記保持手段に書込む書込み手段と、前記保持手段の内容を複数の画素データ列の色情報を格納するメモリセルに転送する手段とを前記画像記憶素子に備えている。

【0010】本発明による他の画像処理装置は、上記の構成のほかに、前記書込み手段による前記色情報可変手段で可変された色情報を前記保持手段に書込む際に外部から指定された画素データの色情報の書込みを禁止する手段を前記画像記憶素子に具備している。

【0011】本発明による別の画像処理装置は、上記の構成のほかに、前記書込み手段による前記色情報可変手

段で可変された色情報を前記保持手段に書込む際に前記色情報を構成するビット情報のうち外部から指定されたビット情報の書込みを禁止する手段を前記画像記憶素子に具備している。

【0012】

【作用】画素データ列のうち指定された描画開始点の画素の色データと、描画終了点の画素の色データとの差と描画画素数とから隣合う画素の可変量を算出し、この可変量を描画開始点の画素の色データに加算する。

【0013】その加算結果を描画開始点の画素の色データが保持されたレジスタの隣のレジスタに保持する。この動作を描画終了点の画素の色データを保持すべきレジスタまで順次繰返し行う。

【0014】これによって、各画素の色データをメモリセルに転送する前にシェーディングを行うことができるので、シェーディングの手法を用いて画像を描画する際に充分な処理速度を得ることができ、部品コスト及び部品実装面積を低減して装置の小型化を可能とすることができる。

【0015】また、色データに可変量を加算してレジスタに書込む際に外部から指定された画素の色データの書込みを禁止することで、シェーディングされた色データに対するラスタ方向のマスクが可能となり、シェーディングされた色データの配置制御が高速化される。

【0016】さらに、色データに可変量を加算してレジスタに書込む際に色データを構成するビット情報のうち外部から指定されたビット情報の書込みを禁止することで、シェーディングされた色データに対するメモリの奥行き方向のマスクが可能となり、シェーディングされた色データ全体に対する明暗等の制御を高速化される。

【0017】

【実施例】次に、本発明の一実施例について図面を参照して説明する。

【0018】図1は本発明の一実施例の構成を示すブロック図である。図において、本発明の一実施例による画像記憶素子は入出力バッファ（Input／OutputBuffer）1と、カウンタ（Counter）2と、ライトデータコントローラ（Write Data Controller）3と、レジスタ群（Register）4と、色データシェーディング演算器（Delta Value& Shade Color Calculator）5と、シリアルライトコントローラ（Serial Write Controller）6と、ライトコントローラ（Write Controller）7と、カラムアドレスレコーダ（Column Decoder）8と、アドレスバッファ（Address Buffer）9と、ロウアドレスデコーダ（Law Decoder）10と、メモリセルアレイ（Memory Cell Array）11と、シリアルアクセスメモリ（Serial Access Mem）12と、シリアル出力バッファ（Serial Output Buffer）13と、ライトマスクレジスタ（Write Mask Register）14と、ライトプレーンマスクコントローラ（Write Plane Mask Controller）15とから構成されている。

【0019】この画像記憶素子において、レジスタ群4は各々8ビット長の色データを保持する256個のレジスタ（レジスタ番号#0～#255）からなり、256通りの異なる8ビット長の色データを保持することができる。ここで、8ビット長の色データ各々は符号無し整数1バイトで表現できる範囲0～255の色値を表している。

【0020】また、色データシェーディング演算器5はレジスタ群4に保持された256通りの異なる8ビット長の色データをシェーディングする機能を持っている。

【0021】上記の画像記憶素子を用いて色データのシェーディングを行う場合、まずレジスタ群4内のレジスタ番号#0～#255の間の任意の隣接しない2つのレジスタに夫々描画開始点及び描画終了点の画素の色データを与える必要がある。

【0022】そこで、シェーディングされた画素の色データの書込みを行う開始点及び終了点のカラムアドレスをカラムアドレスデコーダ8でデコードしてライトデータコントローラ3に出力し、ライトデータコントローラ3によってそれらのカラムアドレスに対応するレジスタ群4のレジスタに描画開始点及び描画終了点各々の画素の色データのみをストアする。

【0023】このシェーディング描画を行う描画画素数は、「（描画終了点のカラムアドレス）－（描画開始点のカラムアドレス）＋1」という計算式からカウンタ2で演算されて保持される。

【0024】色データシェーディング演算器5は描画開始点の色データと描画終了点の色データとを線形補完することでシェーディングを行う。すなわち、色データシェーディング演算器5は描画開始点の色データと描画終了点の色データとの差分を計算し、その差分を描画画素数で割って画素毎に順次累算していく値を求める。

【0025】色データシェーディング演算器5はその求めた値を順次隣合う画素の色データに加算していくことでシェーディングを行う。色データシェーディング演算器5でシェーディングされた画素の色データはライトデータコントローラ3によってレジスタ群4の対応するレジスタに順次書込まれていく。

【0026】レジスタ群4にシェーディング描画を行おうとする画素の色データが全て書込まれると、シリアルライトコントローラ6によってレジスタ群4のデータが最大256画素分同時にメモリセルアレイ11に書込まれる。

【0027】ここで、メモリセルアレイ11は256ビ

ット×５１２のメモリセルが８個で構成されており、これら８個のメモリセル各々には８個のカラムアドレスデコーダ８から夫々カラムアドレスが供給される。

【００２８】一方、入出力バッファ１に接続されたデータバス（図示せず）に、描画開始点及び描画終了点各々の色データとともにラスタ方向のマスクデータを与えた場合、そのマスクデータによってマスクされる色データのレジスタ群４への書込みは禁止される。

【００２９】すなわち、色データシェーディング演算器５でシェーディングされた画素の色データがライトデータコントローラ３によってレジスタ群４の対応するレジスタに書込まれるとき、ライトデータコントローラ３はマスクデータにしたがって対応する色データのレジスタ群４への書込みを禁止する。

【００３０】よって、レジスタ群４からメモリセルアレイ１１にはマスクデータによってマスクされなかった色データのみが転送されることとなる。これによって、表示画面（図示せず）のラスタ方向にシェーディングされた色データの書込みを画素単位で禁止することができる。

【００３１】また、入出力バッファ１に接続されたデータバスに、描画開始点及び描画終了点各々の色データとともにメモリの奥行き方向のマスクデータを与えた場合、色データを構成する８ビットのうちマスクデータによってマスクされるビットに対応する色データのメモリセルアレイ１１への書込みが禁止される。

【００３２】すなわち、データバスから入出力バッファ１に入力されたマスクデータは、入出力バッファ１からライトマスクレジスタ１４にストアされる。ライトプレーンマスクコントローラ１５はレジスタ群４からメモリセルアレイ１１にシェーディングされた色データが転送されるときに、ライトマスクレジスタ１４にストアされているマスクデータに基づき、色データを構成する８ビットのうち対応するビットの色データをレジスタ群４からメモリセルアレイ１１に転送するのを禁止する。これによって、メモリセルアレイ１１の奥行き方向の任意のビットにシェーディングされた色データの書込みを禁止することができる。

【００３３】図２は図１の色データシェーディング演算器５の構成を示すブロック図である。図において、色データシェーディング演算器５は８ビット減算器（８ｂｉｔｓｕｂｂｅｒ）５１と、１６ビット除算器（１６ｂｉｔ ｄｉｖｉｄｅｒ）５２と、１６ビットデータレジスタ（１６ｂｉｔ ｄａｔａ ｒｅｇｉｓｔｅｒ）５３と、１６ビット加算器（１６ ｂｉｔ ａｄｄｅｒ）５４とから構成されている。ここで、１６ビットデータレジスタ５３は内部を整数部８ビット及び小数部８ビットとして使用する。

【００３４】色データシェーディング演算器５は色データをシェーディングする際に、レジスタ群４から与えられた２点（描画開始点及び描画終了点）の画素の色データと描画画素数とに基づいて２点間の色データの差を算出する。

【００３５】すなわち、８ビット減算器５１は描画終了点の色データから描画開始点の色データを引いて、それら２点間の差を算出する。１６ビット除算器５２は８ビット減算器５１で算出された２点間の差を描画画素数で割って２点間の色データの差分△値を算出する。

【００３６】上述したように、２点間の色データの差分△値は、「［（描画終了点の色データ）－（描画開始点の色データ）］／描画画素数」という計算式で求めることができる。この求められた２点間の色データの差分△値は１６ビットデータレジスタ５３に保持される。

【００３７】描画開始点と描画終了点との間の各画素のメモリセルアレイ１１に書込む色データを決定するには、１６ビット加算器５４で描画開始点の色データに２点間の色データの差分△値を加算していくことによって行う。

【００３８】すなわち、レジスタ＃ｎに描画開始点の色データが格納されている場合、このレジスタ＃ｎに格納された色データに１６ビットデータレジスタ５３に保持された差分△値を１６ビット加算器５４で加算し、その値をレジスタ＃（ｎ＋１）に画素の色データとして書込む。

【００３９】また、レジスタ＃（ｎ＋１）の色データに差分△値を加算し、その値をレジスタ＃（ｎ＋２）に画素の色データとして書込むというように、隣のレジスタに保持された色データに差分△値を加算してライトデータコントローラ３の制御でレジスタ群４に順次書込んでいく。ここで、レジスタ群４には計算された色データの整数部８ビットが書込まれる。

【００４０】上記のようにして計算された色データの書込み順序は、（描画開始点の色データが格納されたレジスタ番号）＜（描画終了点の色データが格納されたレジスタ番号）の場合、レジスタ群４の左から右の順となる。

【００４１】一方、（描画開始点の色データが格納されたレジスタ番号）＞（描画終了点の色データが格納されたレジスタ番号）の場合、色データの書込み順序はレジスタ群４の右から左の順となる。

【００４２】例えば、シェーディングされた色データがレジスタ＃２９～＃２２８に格納され、描画開始点の色データをｘ、描画終了点の色データをｙとすると、レジスタ＃３０にはｘ＋（ｘ－ｙ）／２００が、レジスタ＃３１にはｘ＋２［（ｘ－ｙ）／２００］が夫々格納される。

【００４３】以降、レジスタ＃３２～＃２２７に順次差分△値が累算された色データが格納され、レジスタ＃２２８に描画終了点の色データｙが格納されるというように順次△値［（ｘ－ｙ）／２００］が累算されて格納さ

れることになる。

【００４４】したがって、色データシェーディング演算器5に１６ビット加算器５４の加算結果を保持するレジスタと、このレジスタと外部から入力される色データとのうち一方を選択するセレクタとを設けて１６ビット加算器５４の加算結果に順次Δ値を加算していくようにしてもよい。

【００４５】このように、色データのシェーディングを画像記憶素子の内部に設けた色データシェーディング演算器５で行うことによって、色データをシェーディングするための外部のハードウェアが不要となる。

【００４６】よって、シェーディングの手法を用いて画像を描画する際に充分な処理速度を得ることができ、部品コスト及び部品実装面積を低減して装置の小型化を可能とすることができる。

【００４７】また、１回のメモリアクセスで、シェーディングされた色データをラスタ方向に同時に描画することができるので、極めて高速なシェーディング描画を行うことができる。

【００４８】さらに、この１回のメモリアクセスで、シェーディングされた色データに対するラスタ方向またはメモリの奥行き方向のマスクも行うことができるので、シェーディングされた色データの配置やその色データ全体に対する明暗等の制御を高速に行うことができる。

【００４９】

【発明の効果】以上説明したように本発明の画像処理装置によれば、画素データ列のうち指定された画素データ各々の色情報を予め設定された方向に順次可変してレジスタに書込み、このレジスタに書込まれた画素データの色情報をメモリセルに転送することによって、シェーディングの手法を用いて画像を描画する際に充分な処理速度を得ることができ、部品コスト及び部品実装面積を低減して装置の小型化を可能とすることができるという効果がある。

【００５０】また、本発明の他の画像処理装置によれ＊は、可変された画素データの色情報をレジスタに書込む際に外部から指定された画素データの色情報の書込みを禁止することによって、シェーディングされた色情報に対するラスタ方向のマスクを行うことができ、シェーディングされた色データの配置制御を高速化することができるという効果がある。

【００５１】さらに、本発明の別の画像処理装置によれば、可変された画素データの色情報をレジスタに書込む際に色情報を構成するビット情報のうち外部から指定されたビット情報の書込みを禁止することによって、シェーディングされた色情報に対するメモリの奥行き方向のマスクを行うことができ、シェーディングされた色情報全体に対する明暗等の制御を高速化することができるという効果がある。

【図面の簡単な説明】

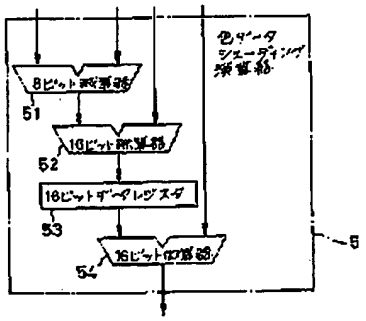
【図１】本発明の一実施例の構成を示すブロック図である。

【図２】図１の色データシェーディング演算器の構成を示すブロック図である。

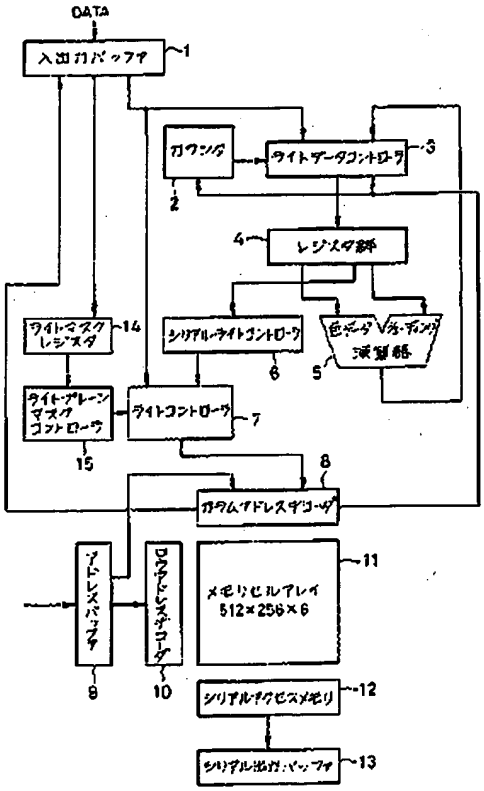
【符号の説明】

２　カウンタ
３　ライトデータコントローラ
４　レジスタ群
５　色データシェーディング演算器
６　シリアルライトコントローラ
７　ライトコントローラ
８　カラムアドレスデコーダ
１１　メモリセルアレイ
１４　ライトマスクレジスタ
１５　ライトプレーンマスクコントローラ
５１　８ビット減算器
５２　１６ビット除算器
５３　１６ビットデータレジスタ
５４　１６ビット加算器

【図２】



【図1】



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CLAIMS

[Claim(s)]

[Claim 1] A maintenance means to be an image processing system containing the image storage element which memorizes the pixel data stream which has color information respectively, and to hold the color information on said pixel data stream, with the color information adjustable means which carries out adjustable [of the color information of each pixel data specified among the color information on the pixel data stream held at said maintenance means] in the direction set up beforehand one by one The image processing system characterized by having the write-in means which writes the color information by which adjustable was carried out with said color information adjustable means in said maintenance means, and a means to transmit the contents of said maintenance means to the memory cell which stores the color information on two or more pixel data streams, in said image storage element.

[Claim 2] The image processing system according to claim 1 characterized by including a means to forbid the writing of the color information on the pixel data specified from the outside when writing the color information by which adjustable was carried out with said color information adjustable means by said write-in means in said maintenance means in said image storage element.

[Claim 3] The image processing system according to claim 1 or 2 characterized by including a means to forbid the writing of the bit information specified from the outside among the bit information which constitutes said color information in case the color information by which adjustable was carried out with said color information adjustable means by said write-in means is written in said maintenance means in said image storage element.

[Claim 4] said color information adjustable means -- the color information on said specified pixel data -- either of claim 1 to claims 3 characterized by to be constituted so that it may carry out adjustable [of the color information of each pixel data between said drawing start point and said point ending / drawing] one by one based on the color information on the pixel data used as the color information on pixel data and the point ending [drawing] which turns into a drawing start point inside -- the image processing system of a publication.

[Claim 5] A subtraction means to perform subtraction with the color information on the pixel data used as the color information on pixel data that said color information adjustable means serves as said drawing start point, and said point ending [drawing], The image processing system according to claim 4 characterized by consisting of a division means which does the division of the subtraction result of said subtraction means with the number of pixels between said drawing start point and said point ending [drawing], and an addition means to add the division result of said division means to the color information on ****** pixel data.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the semi-conductor image storage element used for equipment with the need of writing image data in a memory cell at a high speed about an image processing system.
[0002]
[Description of the Prior Art] Conventionally, in the field of computer graphics, in order to express an image with reality, the shading model is used. This shading model is a method which calculates in approximation whether objective each point is visible to what kind of color and brightness, when a body and the light source are in three-dimensions space.
[0003] That is, when [when the image becomes bright gradually] becoming dark, when the color of an image becomes deep gradually, or when becoming thin, the technique of shading is used in order to express it.
[0004] By the technique of this shading, it has calculated 1 pixel of thickness of the brightness of an image, or a darkness or a color at a time to image data, and that count is performed using software or external hardware.
[0005] The count result of these software or external hardware has memorized every 1 pixel of color data of a pixel in the memory of an image storage element with the address determined to the timing of falling of a row-address strobe signal and a column address strobe signal.
[0006]
[Problem(s) to be Solved by the Invention] Although only the color data of the pixel which it is as a result of [of the software which used the technique of shading, or external hardware] count are memorized in the conventional image storage element mentioned above Software performs the above-mentioned count, and since great count cost starts the above-mentioned count in the case of the approach of memorizing the count result in memory, even if it accelerates the access rate of memory, in case an image is drawn using the technique of shading, sufficient processing speed cannot be obtained.
[0007] Moreover, since great components cost and a large component-side product are required in order for external hardware to perform the above-mentioned count and to perform the above-mentioned count in the case of the approach of memorizing the count result in memory, it has been a serious failure at the time of these miniaturizing equipment.
[0008] Then, it is in the purpose of this invention offering the image processing system which can cancel the above-mentioned trouble, can obtain sufficient processing speed in case an image is drawn using the technique of shading, can reduce components cost and a component-side product, and can enable the miniaturization of equipment.
[0009]
[Means for Solving the Problem] A maintenance means for the image processing system by this invention to be an image processing system containing the image storage element which memorizes the pixel data stream which has color information respectively, and to hold the color information on said pixel data stream, with the color information adjustable means which carries out adjustable [of the color information of each pixel data specified among the color information on the pixel data stream held at said maintenance means] in the direction set up beforehand one by one Said image storage element is equipped with the write-in means which writes the color

information by which adjustable was carried out with said color information adjustable means in said maintenance means, and a means to transmit the contents of said maintenance means to the memory cell which stores the color information on two or more pixel data streams.
[0010] In case other image processing systems by this invention write the color information by which adjustable was carried out with said color information adjustable means by said write-in means in said maintenance means besides the above-mentioned configuration, they possess a means to forbid the writing of the color information on the pixel data specified from the outside, in said image storage element.
[0011] In case another image processing system by this invention writes the color information by which adjustable was carried out with said color information adjustable means by said write-in means in said maintenance means besides the above-mentioned configuration, it possesses a means to forbid the writing of the bit information specified from the outside among the bit information which constitutes said color information, in said image storage element.
[0012]
[Function] The good variate of a ****** pixel is computed from the difference of the color data of the pixel of the drawing start point specified among pixel data streams, and the color data of the pixel of the point ending [drawing], and the number of drawing pixels, and this good variate is added to the color data of the pixel of a drawing start point.
[0013] The addition result is held to the register of the next door of the register with which the color data of the pixel of a drawing start point were held. Even the register which should hold the color data of the pixel of the point ending [drawing] performs this actuation repeatedly one by one.
[0014] By this, since shading can be performed before transmitting the color data of each pixel to a memory cell, in case an image is drawn using the technique of shading, sufficient processing speed can be obtained, components cost and a component-side product can be reduced, and the miniaturization of equipment can be enabled.
[0015] Moreover, the mask of the direction of a raster to the color data by which shading was carried out becomes possible by forbidding the writing of the color data of the pixel specified from the outside, in case a good variate is added to color data and it writes in a register, and the configuration control of color data by which shading was carried out is accelerated.
[0016] Furthermore, MASUKUGA of the depth direction of the memory to the color data by which shading was carried out becomes possible by forbidding the writing of the bit information specified from the outside among the bit information which constitutes color data, in case a good variate is added to color data and it writes in a register, and control of the light and darkness to the whole color data by which shading was carried out etc. is accelerated.
[0017]
[Example] Next, one example of this invention is explained with reference to a drawing.
[0018] Drawing 1 is the block diagram showing the configuration of one example of this invention. In drawing, the image storage element by one example of this invention An input output buffer 1 (Input/OutputBuffer), A counter (Counter) 2 and the light data controller 3 (Write Data Controller), The register group (Register) 4 and the color data shading computing element 5 (Delta Value& Shade Color Calculator), The serial light controller 6 (Serial Write Controller), The light controller 7 (Write Controller), The column address recorder 8 (Column Decoder), An address buffer (Address Buffer) 9 and the row address decoder 10 (Law Decoder), The memory cell array 11 (Memory Cell Array), Serial access memory 12 (Serial Access Mem), The serial output buffer 13 (Serial Output Buffer), It consists of a light mask register (Write Mask Register)

14 and a light plane mask controller (Write Plane Mask Controller) 15.
[0019] In this image storage element, the register group 4 consists of 256 registers (register number #0-#255) which hold the color data of 8 bit length respectively, and can hold the color data of 256 kinds of different 8 bit length. Here, the color data of each of 8 bit length express the color value of the range 0-255 which can be expressed for the sign-less integer of 1 byte.
[0020] Moreover, the color data shading computing element 5 has the function which carries out shading of the color data of 256 kinds held at the register group 4 of different 8 bit length.
[0021] When performing shading of color data using the above-mentioned image storage element, it is necessary to give the color data of the pixel of a drawing start point and the point ending [drawing] to two registers with which the arbitration between register number #0-#255 in the register group 4 does not adjoin probably, respectively.
[0022] then, the column address of the start point which writes in the color data of the pixel by which shading was carried out, and an ending point is decoded by the column address decoder 8, it outputs to the light data controller 3, and only a drawing start point and the color data of the pixel of each point ending [drawing] are stored in the register of the register group 4 corresponding to those column addresses by the light data controller 3.
[0023] The number of drawing pixels which performs this shading drawing is calculated and held with a counter 2 from the formula "-(column address of the point ending [drawing]) (column address of a drawing start point) 1 [+]."
[0024] The color data shading computing element 5 performs shading by carrying out the linearity complement of the color data of a drawing start point, and the color data of the point ending [drawing]. That is, the color data shading computing element 5 calculates the difference of the color data of a drawing start point, and the color data of the point ending [drawing], and calculates the value which divides the difference by the number of drawing pixels, and carries out sequential accumulation for every pixel.
[0025] The color data shading computing element 5 performs shading by adding the calculated value to the color data of a ****** pixel one by one. The color data of the pixel by which shading was carried out with the color data shading computing element 5 are written in the register to which the register group 4 corresponds by the light data controller 3 one by one.
[0026] If all the color data of the pixel which is going to perform shading drawing in the register group 4 are written in, the data of the register group 4 will be written in coincidence by a maximum of 256 pixels by the serial light controller 6 at the memory cell array 11.
[0027] Here, the memory cell of 256 bit x512 consists of eight pieces, and, as for the memory cell array 11, a column address is supplied to these eight memory cells of each from eight column address decoders 8, respectively.
[0028] on the other hand, when the mask data of the direction of a raster are given to the data bus (not shown) connected to the input output buffer 1 with a drawing start point and the color data of each point ending [drawing], the writing to the register group 4 of the color data by which a mask is carried out with the mask data is forbidden.
[0029] That is, when the color data of the pixel by which shading was carried out with the color data shading computing element 5 are written in the register to which the register group 4 corresponds by the light data controller 3, the light data controller 3 forbids the writing to the register group 4 of the color data which correspond according to mask data.
[0030] Therefore, only the color data by which a mask was not carried out with mask data will be transmitted to the memory cell array 11 from the register group 4. By this, the writing of color data by which shading was carried out in the direction of a raster of a display screen (not shown)

can be forbidden per pixel.
[0031] moreover, when the mask data of the depth direction of memory are given to the data bus connected to the input output buffer 1 with a drawing start point and the color data of each point ending [drawing], the writing to the memory cell array 11 of the color data corresponding to the bit by which a mask is carried out with mask data among 8 bits which constitutes color data is forbidden.
[0032] That is, the mask data inputted into the input output buffer 1 from the data bus are stored in the light mask register 14 from an input output buffer 1. The light plane mask controller 15 is forbidden from transmitting the color data of a bit which correspond among 8 bits which constitutes color data from the register group 4 to the memory cell array 11 based on the mask data currently stored in the light mask register 14, when the color data by which shading was carried out to the memory cell array 11 from the register group 4 are transmitted. By this, the writing of color data by which shading was carried out to the bit of the arbitration of the depth direction of the memory cell array 11 can be forbidden.
[0033] Drawing 2 is the block diagram showing the configuration of the color data shading computing element 5 of drawing 1 . In drawing, the color data shading computing element 5 consists of the 8-bit subtractor (8 bitsubber) 51, a 16-bit divider (16 bit divider) 52, a 16-bit data register (16 bit data register) 53, and a 16-bit adder (16 bit adder) 54. Here, the 16-bit data register 53 uses the interior as 8 bits of integer part, and 8 bits of fraction part.
[0034] In case the color data shading computing element 5 carries out shading of the color data, it computes the difference of the color data for two points based on the color data and the number of drawing pixels of the pixel of two points (a drawing start point and point ending [drawing]) which were given from the register group 4.
[0035] Namely, the 8-bit subtractor 51 computes the difference for these two points by lengthening the color data of a drawing start point from the color data of the point ending [drawing]. the difference for two points by which the 16-bit divider 52 was computed with the 8-bit subtractor 51 -- the number of drawing pixels -- dividing -- the difference of the color data for two points -- delta value is computed.
[0036] it mentioned above -- as -- the difference of the color data for two points -- delta value can be calculated in the formula "[(color data of the point ending [drawing]) - (color data of a drawing start point)] / the number of drawing pixels." the difference of the color data for these two points searched for -- delta value is held at the 16-bit data register 53.
[0037] for determining the color data written in the memory cell array 11 of each pixel between a drawing start point and the point ending [drawing] -- the 16-bit adder 54 -- the color data of a drawing start point -- the difference of the color data for two points -- it carries out by adding delta value.
[0038] namely, the difference held at the 16-bit data register 53 at the color data stored in this register #n when the color data of a drawing start point were stored in register #n -- delta value is added with the 16-bit adder 54, and that value is written in register # (n+1) as color data of a pixel.
[0039] moreover, the color data of register # (n+1) -- difference -- the color data held at the next register as delta value was added and the value was written in register # (n+2) as color data of a pixel -- difference -- delta value is added and it writes in the register group 4 one by one by control of the light data controller 3. Here, 8 bits of integer part of the calculated color data are written in the register group 4.
[0040] the write-in sequence of the color data calculated as mentioned above -- < (register

number in which the color data of a drawing start point were stored) (register number in which the color data of the point ending [drawing] were stored) -- it is -- a case -- the register group 4 -- it becomes right order from the left.
[0041] On the other hand, when it is > (register number in which the color data of a drawing start point were stored) (register number in which the color data of the point ending [drawing] were stored), the write-in sequence of color data serves as left order from the right of the register group 4.
[0042] For example, when the color data by which shading was carried out are stored in register #29-#228 and set the color data of x and the point ending [drawing] to y for the color data of a drawing start point, x+ (x-y) / 200 are stored in register #30, and x+2 [(x-y) /200] is stored in register #31, respectively.
[0043] register #32-#227 [henceforth,] -- one by one -- difference -- one by one, delta value [(x-y) /200] will accumulate and will be stored as the color data which ** value accumulated are stored and the color data y of the point ending [drawing] are stored in register #228.
[0044] Therefore, the selector which chooses one side among the color data inputted into the color data shading computing element 5 from the register holding the addition result of the 16-bit adder 54, this register, and the outside is prepared, and you may make it add delta value to the addition result of the 16-bit adder 54 one by one.
[0045] Thus, the hardware of the exterior for carrying out shading of the color data becomes unnecessary by performing shading of color data with the color data shading computing element 5 formed in the interior of an image storage element.
[0046] Therefore, in case an image is drawn using the technique of shading, sufficient processing speed can be obtained, components cost and a component-side product can be reduced, and the miniaturization of equipment can be enabled.
[0047] Moreover, since the color data by which shading was carried out can be drawn in the direction of a raster by one memory access at coincidence, very high-speed shading drawing can be performed.
[0048] Furthermore, since the mask of the direction of a raster over the color data by which shading was carried out, or the depth direction of memory can also be performed, the light and darkness to the arrangement of color data by which shading was carried out, or its whole color data etc. are controllable by this one memory access at a high speed.
[0049]
[Effect of the Invention] The writing [as explained above, carry out adjustable / of the color information of each pixel data which was specified among pixel data streams according to the image processing system of this invention / in the direction set up beforehand one by one, and] to a register By transmitting the color information on the pixel data written in this register to a memory cell In case an image is drawn using the technique of shading, sufficient processing speed can be obtained, and it is effective in the ability to reduce components cost and a component-side product, and enable the miniaturization of equipment.
[0050] Moreover, in case the color information on the pixel data by which adjustable was carried out is written in a register according to other image processing systems of this invention, by forbidding the writing of the color information on the pixel data specified from the outside, the mask of the direction of a raster to the color information by which shading was carried out can be performed, and it is effective in the configuration control of color data by which shading was carried out being accelerable.
[0051] Furthermore, by forbidding the writing of the bit information specified from the outside

among the bit information which constitutes color information in case the color information on the pixel data by which adjustable was carried out is written in a register according to another image processing system of this invention The mask of the depth direction of memory to the color information by which shading was carried out can be performed, and it is effective in control of the light and darkness to the whole color information by which shading was carried out etc. being accelerable.

TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the semi-conductor image storage element used for equipment with the need of writing image data in a memory cell at a high speed about an image processing system.

PRIOR ART

[Description of the Prior Art] Conventionally, in the field of computer graphics, in order to express an image with reality, the shading model is used. This shading model is a method which calculates in approximation whether objective each point is visible to what kind of color and brightness, when a body and the light source are in three-dimensions space.
[0003] That is, when [when the image becomes bright gradually] becoming dark, when the color of an image becomes deep gradually, or when becoming thin, the technique of shading is used in order to express it.
[0004] By the technique of this shading, it has calculated 1 pixel of thickness of the brightness of an image, or a darkness or a color at a time to image data, and that count is performed using software or external hardware.
[0005] The count result of these software or external hardware has memorized every 1 pixel of color data of a pixel in the memory of an image storage element with the address determined to the timing of falling of a row-address strobe signal and a column address strobe signal.

EFFECT OF THE INVENTION

[Effect of the Invention] as explained above, according to the image processing system of this invention, carry out adjustable [of the color information of each pixel data specified among pixel data streams] in the direction set up beforehand one by one By transmitting the color information on the pixel data written in the register at writing and this register to a memory cell, in case an image is drawn using the technique of shading, sufficient processing speed can be obtained, and it is effective in the ability to reduce components cost and a component-side product, and enable the miniaturization of equipment.
[0050] Moreover, in case the color information on the pixel data by which adjustable was carried out is written in a register according to other image processing systems of this invention, by forbidding the writing of the color information on the pixel data specified from the outside, the mask of the direction of a raster to the color information by which shading was carried out can be

performed, and it is effective in the configuration control of color data by which shading was carried out being accelerable.
[0051] Furthermore, the thing for which the writing of the bit information specified from the outside among the bit information which constitutes color information is forbidden in case the color information on the pixel data by which adjustable was carried out is written in a register according to another image processing system of this invention, The mask of the depth direction of memory to the color information by which shading was carried out can be performed, and it is effective in control of the light and darkness to the whole color information by which shading was carried out etc. being accelerable.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although only the color data of the pixel which it is as a result of [of the software which used the technique of shading, or external hardware] count are memorized in the conventional image storage element mentioned above Software performs the above-mentioned count, and since great count cost starts the above-mentioned count in the case of the approach of memorizing the count result in memory, even if it accelerates the access rate of memory, in case an image is drawn using the technique of shading, sufficient processing speed cannot be obtained.
[0007] Moreover, since great components cost and a large component-side product are required in order for external hardware to perform the above-mentioned count and to perform the above-mentioned count in the case of the approach of memorizing the count result in memory, it has been a serious failure at the time of these miniaturizing equipment.
[0008] Then, it is in the purpose of this invention offering the image processing system which can cancel the above-mentioned trouble, can obtain sufficient processing speed in case an image is drawn using the technique of shading, can reduce components cost and a component-side product, and can enable the miniaturization of equipment.

MEANS

[Means for Solving the Problem] A maintenance means for the image processing system by this invention to be an image processing system containing the image storage element which memorizes the pixel data stream which has color information respectively, and to hold the color information on said pixel data stream, with the color information adjustable means which carries out adjustable [of the color information of each pixel data specified among the color information on the pixel data stream held at said maintenance means] in the direction set up beforehand one by one Said image storage element is equipped with the write-in means which writes the color information by which adjustable was carried out with said color information adjustable means in said maintenance means, and a means to transmit the contents of said maintenance means to the memory cell which stores the color information on two or more pixel data streams.
[0010] In case other image processing systems by this invention write the color information by which adjustable was carried out with said color information adjustable means by said write-in means in said maintenance means besides the above-mentioned configuration, they possess a

means to forbid the writing of the color information on the pixel data specified from the outside, in said image storage element.
[0011] In case another image processing system by this invention writes the color information by which adjustable was carried out with said color information adjustable means by said write-in means in said maintenance means besides the above-mentioned configuration, it possesses a means to forbid the writing of the bit information specified from the outside among the bit information which constitutes said color information, in said image storage element.

OPERATION

[Function] The good variate of a ****** pixel is computed from the difference of the color data of the pixel of the drawing start point specified among pixel data streams, and the color data of the pixel of the point ending [drawing], and the number of drawing pixels, and this good variate is added to the color data of the pixel of a drawing start point.
[0013] The addition result is held to the register of the next door of the register with which the color data of the pixel of a drawing start point were held. Even the register which should hold the color data of the pixel of the point ending [drawing] performs this actuation repeatedly one by one.
[0014] By this, since shading can be performed before transmitting the color data of each pixel to a memory cell, in case an image is drawn using the technique of shading, sufficient processing speed can be obtained, components cost and a component-side product can be reduced, and the miniaturization of equipment can be enabled.
[0015] Moreover, the mask of the direction of a raster to the color data by which shading was carried out becomes possible by forbidding the writing of the color data of the pixel specified from the outside, in case a good variate is added to color data and it writes in a register, and the configuration control of color data by which shading was carried out is accelerated.
[0016] Furthermore, MASUKUGA of the depth direction of the memory to the color data by which shading was carried out becomes possible by forbidding the writing of the bit information specified from the outside among the bit information which constitutes color data, in case a good variate is added to color data and it writes in a register, and control of the light and darkness to the whole color data by which shading was carried out etc. is accelerated.

EXAMPLE

[Example] Next, one example of this invention is explained with reference to a drawing.
[0018] Drawing 1 is the block diagram showing the configuration of one example of this invention. In drawing, the image storage element by one example of this invention An input output buffer 1 (Input/OutputBuffer), A counter (Counter) 2 and the light data controller 3 (Write Data Controller), The register group (Register) 4 and the color data shading computing element 5 (Delta Value& Shade Color Calculator), The serial light controller 6 (Serial Write Controller), The light controller 7 (Write Controller), The column address recorder 8 (Column Decoder), An address buffer (Address Buffer) 9 and the row address decoder 10 (Law Decoder), The memory cell array 11 (Memory Cell Array), Serial access memory 12 (Serial Access Mem), The serial

output buffer 13 (Serial Output Buffer), It consists of a light mask register (Write Mask Register) 14 and a light plane mask controller (Write Plane Mask Controller) 15.
[0019] In this image storage element, the register group 4 consists of 256 registers (register number #0-#255) which hold the color data of 8 bit length respectively, and can hold the color data of 256 kinds of different 8 bit length. Here, the color data of each of 8 bit length express the color value of the range 0-255 which can be expressed for the sign-less integer of 1 byte.
[0020] Moreover, the color data shading computing element 5 has the function which carries out shading of the color data of 256 kinds held at the register group 4 of different 8 bit length.
[0021] When performing shading of color data using the above-mentioned image storage element, it is necessary to give the color data of the pixel of a drawing start point and the point ending [drawing] to two registers with which the arbitration between register number #0-#255 in the register group 4 does not adjoin probably, respectively.
[0022] then, the column address of the start point which writes in the color data of the pixel by which shading was carried out, and an ending point is decoded by the column address decoder 8, it outputs to the light data controller 3, and only a drawing start point and the color data of the pixel of each point ending [drawing] are stored in the register of the register group 4 corresponding to those column addresses by the light data controller 3.
[0023] The number of drawing pixels which performs this shading drawing is calculated and held with a counter 2 from the formula "-(column address of the point ending [drawing]) (column address of a drawing start point) 1 [+]."
[0024] The color data shading computing element 5 performs shading by carrying out the linearity complement of the color data of a drawing start point, and the color data of the point ending [drawing]. That is, the color data shading computing element 5 calculates the difference of the color data of a drawing start point, and the color data of the point ending [drawing], and calculates the value which divides the difference by the number of drawing pixels, and carries out sequential accumulation for every pixel.
[0025] The color data shading computing element 5 performs shading by adding the calculated value to the color data of a ****** pixel one by one. The color data of the pixel by which shading was carried out with the color data shading computing element 5 are written in the register to which the register group 4 corresponds by the light data controller 3 one by one.
[0026] If all the color data of the pixel which is going to perform shading drawing in the register group 4 are written in, the data of the register group 4 will be written in coincidence by a maximum of 256 pixels by the serial light controller 6 at the memory cell array 11.
[0027] Here, the memory cell of 256 bit x512 consists of eight pieces, and, as for the memory cell array 11, a column address is supplied to these eight memory cells of each from eight column address decoders 8, respectively.
[0028] on the other hand, when the mask data of the direction of a raster are given to the data bus (not shown) connected to the input output buffer 1 with a drawing start point and the color data of each point ending [drawing], the writing to the register group 4 of the color data by which a mask is carried out with the mask data is forbidden.
[0029] That is, when the color data of the pixel by which shading was carried out with the color data shading computing element 5 are written in the register to which the register group 4 corresponds by the light data controller 3, the light data controller 3 forbids the writing to the register group 4 of the color data which correspond according to mask data.
[0030] Therefore, only the color data by which a mask was not carried out with mask data will be transmitted to the memory cell array 11 from the register group 4. By this, the writing of color

data by which shading was carried out in the direction of a raster of a display screen (not shown) can be forbidden per pixel.
[0031] moreover, when the mask data of the depth direction of memory are given to the data bus connected to the input output buffer 1 with a drawing start point and the color data of each point ending [drawing], the writing to the memory cell array 11 of the color data corresponding to the bit by which a mask is carried out with mask data among 8 bits which constitutes color data is forbidden.
[0032] That is, the mask data inputted into the input output buffer 1 from the data bus are stored in the light mask register 14 from an input output buffer 1. The light plane mask controller 15 is forbidden from transmitting the color data of a bit which correspond among 8 bits which constitutes color data from the register group 4 to the memory cell array 11 based on the mask data currently stored in the light mask register 14, when the color data by which shading was carried out to the memory cell array 11 from the register group 4 are transmitted. By this, the writing of color data by which shading was carried out to the bit of the arbitration of the depth direction of the memory cell array 11 can be forbidden.
[0033] Drawing 2 is the block diagram showing the configuration of the color data shading computing element 5 of drawing 1 . In drawing, the color data shading computing element 5 consists of the 8-bit subtractor (8 bitsubber) 51, a 16-bit divider (16 bit divider) 52, a 16-bit data register (16 bit data register) 53, and a 16-bit adder (16 bit adder) 54. Here, the 16-bit data register 53 uses the interior as 8 bits of integer part, and 8 bits of fraction part.
[0034] In case the color data shading computing element 5 carries out shading of the color data, it computes the difference of the color data for two points based on the color data and the number of drawing pixels of the pixel of two points (a drawing start point and point ending [drawing]) which were given from the register group 4.
[0035] Namely, the 8-bit subtractor 51 computes the difference for these two points by lengthening the color data of a drawing start point from the color data of the point ending [drawing]. the difference for two points by which the 16-bit divider 52 was computed with the 8-bit subtractor 51 -- the number of drawing pixels -- dividing -- the difference of the color data for two points -- delta value is computed.
[0036] it mentioned above -- as -- the difference of the color data for two points -- delta value can be calculated in the formula "[(color data of the point ending [drawing]) - (color data of a drawing start point)] / the number of drawing pixels." the difference of the color data for these two points searched for -- delta value is held at the 16-bit data register 53.
[0037] for determining the color data written in the memory cell array 11 of each pixel between a drawing start point and the point ending [drawing] -- the 16-bit adder 54 -- the color data of a drawing start point -- the difference of the color data for two points -- it carries out by adding delta value.
[0038] namely, the difference held at the 16-bit data register 53 at the color data stored in this register #n when the color data of a drawing start point were stored in register #n -- delta value is added with the 16-bit adder 54, and that value is written in register # (n+1) as color data of a pixel.
[0039] moreover, the color data of register # (n+1) -- difference -- the color data held at the next register as delta value was added and the value was written in register # (n+2) as color data of a pixel -- difference -- delta value is added and it writes in the register group 4 one by one by control of the light data controller 3. Here, 8 bits of integer part of the calculated color data are written in the register group 4.

[0040] the write-in sequence of the color data calculated as mentioned above -- < (register number in which the color data of a drawing start point were stored) (register number in which the color data of the point ending [drawing] were stored) -- it is -- a case -- the register group 4 -- it becomes right order from the left.
[0041] On the other hand, when it is > (register number in which the color data of a drawing start point were stored) (register number in which the color data of the point ending [drawing] were stored), the write-in sequence of color data serves as left order from the right of the register group 4.
[0042] For example, when the color data by which shading was carried out are stored in register #29-#228 and set the color data of x and the point ending [drawing] to y for the color data of a drawing start point, x+ (x-y) / 200 are stored in register #30, and x+2 [(x-y) /200] is stored in register #31, respectively.
[0043] register #32-#227 [henceforth,] -- one by one -- difference -- one by one, delta value [(x-y) /200] will accumulate and will be stored as the color data which ** value accumulated are stored and the color data y of the point ending [drawing] are stored in register #228.
[0044] Therefore, the selector which chooses one side among the color data inputted into the color data shading computing element 5 from the register holding the addition result of the 16-bit adder 54, this register, and the outside is prepared, and you may make it add delta value to the addition result of the 16-bit adder 54 one by one.
[0045] Thus, the hardware of the exterior for carrying out shading of the color data becomes unnecessary by performing shading of color data with the color data shading computing element 5 formed in the interior of an image storage element.
[0046] Therefore, in case an image is drawn using the technique of shading, sufficient processing speed can be obtained, components cost and a component-side product can be reduced, and the miniaturization of equipment can be enabled.
[0047] Moreover, since the color data by which shading was carried out can be drawn in the direction of a raster by one memory access at coincidence, very high-speed shading drawing can be performed.
[0048] Furthermore, since the mask of the direction of a raster over the color data by which shading was carried out, or the depth direction of memory can also be performed, the light and darkness to the arrangement of color data by which shading was carried out, or its whole color data etc. are controllable by this one memory access at a high speed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of one example of this invention.
[Drawing 2] It is the block diagram showing the configuration of the color data shading computing element of drawing 1 .
[Description of Notations]
2 Counter
3 Light Data Controller
4 Register Group
5 Color Data Shading Computing Element
6 Serial Light Controller

7 Light Controller
8 Column Address Decoder
11 Memory Cell Array
14 Light Mask Register
15 Light Plane Mask Controller
51 8-Bit Subtractor
52 16-Bit Divider
53 16-Bit Data Register
54 16-Bit Adder